bitvis

Quality in every bit

Embedded systems
SW FPGA ASIC

A new design centre for FPGA and Embedded SW

Investing in improvements

- Analysing delays, problems and deficiencies
- Regular workshops on pitfalls and improvement potentials
- Sharing experience
- Making tools and IP for faster and safer product development
- Improving and coordinating the design flow from A to Z

Better Designers

- Focus on design structure, layering, readability and modifiability
- Awareness of pitfalls and mitigations
- Knowledge of critical challenges
- Getting vital experience faster
- Skilled in verification & test
- Trained in Bitvis methodology, tools and IP
- Robust designs

Better Methodology, Tools, IP

- FPGA simulation booster though testbench simplification
  - Bitvis testbench utilities
  - Bitvis TLM system
- SW / FPGA co-design support
  - Register Wizard
- FPGA Development Best Practises
  - 2-day course. Very good feedback
  - On-site variants on request
  - Used internally on a regular basis

Better Projects & Products

- Better product quality and lower risk
- Reduced time to fully functional design
- Better/simpler handover
- Easier to modify in the future
- No need for “legacy consultants”
- Lower total development cost
- Lower total product cost and LCC
- May help customers improve their knowledge and methodology

Quality of service rather than dependency

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