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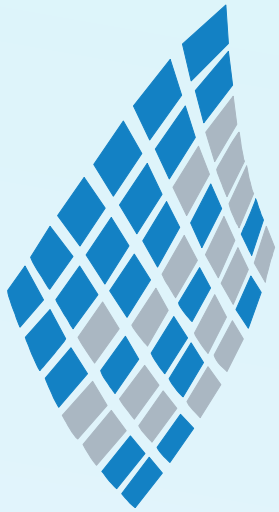
More info on 'FPGA Development Best Practices'



Your partner for SW and FPGA (& ASIC)

FPGA Development Best Practices

- Two-day course
  - In Denmark, Norway and Sweden - so far
  - Main focus:
    Practical Quality and Efficiency improvement
    - making you a better designer
    - allowing faster development and better quality products
  - Pragmatic approach to problems and challenges:
    Design flow, conventions, checklists, documentation, pitfalls, reviews, simple and advanced verification, testbench support, simple and advanced clocking and timing, design structuring and readability, bus systems, plug'n'play reuse, modified reuse, flexibility, simple and advanced synchronization, delta cycle problems, project and technical management, etc…
- On-site variants of this course on demand

Scope

- Main focus will be:
  - Significantly improving FPGA development efficiency
  - Reducing Risk & Improving Quality
  - Best practices & Practical industrial experience
  - Pragmatic approach
    - Simple and low cost solutions that can be applied today
    - Shows how you can implement a good reuse methodology, step by step; – steadily improving your efficiency and quality

Focus: Faster, Cheaper & Safer FPGA Development

Equally relevant for large and small companies

Target Audience and Prerequisites Day 1

Target audience:

- Any FPGA designer who wants to be more structured
- Any FPGA designer who wants to implement a good design flow and important quality improvement aspects
- Technical managers and coordinators with FPGA-related responsibilities who wants to improve FPGA-based product development and introduce a common, structured design flow
- Project managers for projects including FPGAs or internal FPGA-related deliveries

Prerequisites:

- A good understanding of digital design
- Experience from FPGA development
  - As a designer, coordinator or project/line manager

(Note: 95% of the course is equally relevant for Digital ASIC)

Target Audience and Prerequisites Day 2

Target audience:

- Experienced FPGA designers
  - who want to be more structured and design better products
  - who want a better overview of improvement potentials
- Technical managers and coordinators with FPGA experience
  - who want their FPGA team to work better
  - who want to have a uniform development flow and methodology

Prerequisites:

- A good understanding of digital design
- A good basic understanding of FPGA development problem areas
  - Design, timing, clocking, reuse, verification, quality assurance
- Experience from multiple FPGA projects
  - As a designer, coordinator or project/line manager

(Note: 95% of the course is equally relevant for Digital ASIC)

Main subjects

Approximate split on main subjects:

- 35%
  Design – architecture, structure, issues, coding
- 25%
  Verification – architecture, structure, methodology
- 20%
  Clocking, Clock Domain crossing, Resets and Timing
- 10%
  Reuse and design for reuse
- 10%
  Quality assurance – at the development level

About the presenter

- Espen Tallaksen, Bitvis AS, Norway
  - Previous work experience: *Autodisplay, Kongsberg Defence Communication, Philips Semiconductors (Zuerich), Nordic VLSI, Digitas and Data Respons*
  - Experience : 25 years (Digital, FPGA, ASIC)
  - Has performed development, methodology build-up and efficiency improvement for several companies.
  - Methodology responsible at Digitas
    - Architecture, Specification, Design & Verification
    - Design and Verification efficiency improvement
    - Implementation and project coordination
    - Focus on structured approach and efficient reuse.
  - Technology Manager at Data Respons, Norway
    - Methodology improvements coordinator
  - *Applies a pragmatic approach to efficiency & quality improvement*

Previous Courses and Presentations

- This course several times since 2008 in Scandinavia
- "Faster, Cheaper and Safer FPGA development"
  - Keynote at FPGAworld, Stockholm 2005
- Various presentations on
  - Design, Reuse and Efficiency
  - Verification methodology and Testbench Reuse
  - Best Practices (Design, Clocking, Timing, Reuse, Verfication, etc.)
- Presented at various seminars and locations
  - FPGAworld, Stockholm
  - Mentor Expo, Stockholm
  - FPGA-forum, Trondheim
  - and at various companies
    - ABB, Adva Optical, Ericsson, FOI (Sweden), Kongsberg, Norspace, ProjectionDesign, Tomra, Tandberg, GE Healthcare, Vingmed, WesternGeco and several others

Misc

- Focus in this course is on efficiency & quality – through improved awareness, knowledge, competence and experience
  - The course is FPGA technology independent
  - The course is tool independent
  - The course is mainly language independent
    - But – VDHL will be used in examples
    - and – some VHDL coding and flexibility issues will be presented.
- PDF handouts will be given for all PowerPoint slides presented

What will you gain from this course?

- After this course you will:
  - Have an overview of:
    - General FPGA efficiency & quality improvement potentials
    - The most important structural issues to resolve
    - Why planned reuse is so much better than ad-hoc reuse
    - How to avoid common pitfalls and secure sufficient quality
    - Important development issues – on which to focus
      - Design, Timing, Clocking, Analysis, Verification, Structure
    - How you should plan and prioritize your improvement steps
  - Have inspiration and new ideas for:
    - How your company can improve
    - How you can improve as an FPGA-related manager
    - How your FPGA team can work far better together
    - How you can become a better designer

End

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We are a team of very dedicated and experienced designers
who have chosen to specialize in developing embedded SW and FPGA;
because this is what we do best,
- but even more important
– because we enjoy it.

A partner
for SW and FPGA (& ASIC)